

Cray XT5_h™ Supercomputer



Cray XT5_h System Highlights

New generations of scalar microprocessors have continually offered higher clock rates in accordance with Moore's Law, but growing power and heat issues have stopped that trend, thus diminishing the overall performance gains offered by even the most powerful scalar processors. Increasingly, users who need a significant boost in application performance are turning to alternative processor architectures that can extract greater parallelism from application codes.

Recognizing that no single architecture is ideally suited for all types of applications, Cray introduces the industry's first hybrid supercomputer that can integrate multiple processor architectures into a single system and accelerate high performance computing (HPC) workflows — the Cray XT5_h supercomputer.

Optimizes High Performance Workflows

The Cray XT5_h supercomputer surpasses the capabilities of commodity microprocessors by delivering higher sustained performance, by applying alternative processor architectures across select applications within a HPC workflow. The Cray XT5_h architecture supports a variety of processor technologies, including scalar processors based on AMD Opteron™ dual and quad-core technologies, vector processors, and FPGA accelerators.

High Memory Bandwidth and Large Global Address Space

Offers 28.5 GBytes/sec of memory bandwidth and supports 1024 processors addressing 16 Terabytes of physical memory.

Most Advanced Parallel Programming Languages

The Cray XT5_h system has unique global addressing capabilities programmable by Co-Array Fortran (CAF) and Unified Parallel C (UPC) which can solve problems beyond the capabilities of MPI.

Significant Step in Adaptive Supercomputing

The Cray XT5_h marks a milestone on the path to Adaptive Supercomputing, Cray's vision for innovative next-generation products that integrate diverse processing technologies into a unified architecture, surpassing today's limitations and meeting the market's continued demand for realized performance.

Cray XT5_h Supercomputer

The Cray XT5_h supercomputer can integrate multiple processor architectures into a single system accelerating the most demanding computational workflows. Coupling industry-leading scalar processing capability with high-bandwidth vector processing and reconfigurable FPGA acceleration, the Cray XT5_h system establishes a new paradigm in high performance computing.

With a proven and mature programming environment for vector processors, programs can be written in C or Fortran and compiled directly to the vector processors, a capability that doesn't exist today for other accelerators.

Optimizing HPC Workflows

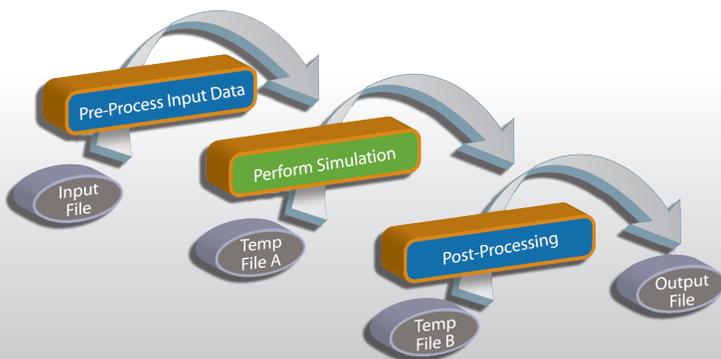
The Cray XT5_h system augments the capabilities of today's multi-core processors by delivering higher sustained performance across a variety of applications within an HPC workflow improving time to solution and increasing competitiveness.

Complex high performance workflows consist of both scalar applications with "cache-friendly" memory access patterns, and more memory-intensive workloads with massive data volumes to process, often with unpredictable access patterns. These types of complex workflows can never achieve optimal performance relying completely on a single, scalar multi-core architecture, but may be ideal candidates for vector processing or targeted FPGA acceleration.

The Cray XT5_h hybrid supercomputer is the industry's first supercomputer that can support any or all of these processor architectures within a single system.

Cray XT5_h HPC Workflow

Here, the first part of the workflow consists of a scalar-dominated application which performs best on the scalar nodes of the Cray XT5_h system. The system sends the output to another application whose memory-intensive workload and massive data volumes run best on the system's vector nodes. Finally, the system calls another application to complete the workflow on the system's scalar nodes—resulting in shorter overall processing time than if the workflow ran on either an all-scalar or all-vector system.



- Scalar
- Vector

Hybrid Software Environment

The Cray XT5_h supercomputer provides an established and complete software development environment to harness the full power of the system's hybrid supercomputing capabilities. This environment includes proven and powerful vector compilers, scientific and math libraries, debuggers, and performance analysis tools.

The Cray XT5_h system runs a Linux environment, providing a single point of login across all system resources or blades. A common Application Level Placement Scheduler (ALPS) allows for simplified application scheduling across the system's scalar, vector, and FPGA blades. The scheduler also fully integrates with workload management applications including PBS Pro and LSF, guaranteeing resource availability for batch and interactive requests.

A Lustre[®] file system provides shared file access of common input and output files to all applications and computational resources in the workflow. Applications can easily and immediately access the output of one application from one resource as the input to another application within the workflow. Socket-based communication between applications also facilitates advanced hybrid application development.

Advanced Parallel Programming Languages

The Cray XT5_h system supports the Parallel Global Address Space (PGAS) Languages, Co-Array Fortran (CAF) and Unified Parallel C (UPC). These allow programmers to specify both data distribution and work distribution in a single program multiple data (SPMD) programming model. These advanced languages are not supported on distributed memory clusters. CAF and UPC can be used as an alternative to message-passing methods such as MPI and SHMEM.

With co-arrays, the concept of a (logical) processor is replaced by the concept of an image. When data objects are declared as part of a co-array, data on different images can be read or written in a fashion similar to the way in which arrays are read and written in Fortran.

Co-arrays offer the following advantages:

- Co-arrays are syntax-based, so programs that use them can be analyzed and optimized by the compiler. This offers a much greater opportunity for hiding data transfer latency, since references to remote memory locations can be pipelined.
- Co-array syntax can eliminate the need to create and copy data to local temporary arrays.
- Co-arrays express data transfer naturally through the syntax of the language, making the code more readable and maintainable.

UPC is a parallel extension of the C programming language also used with multiprocessors with a common global address space. The purpose of UPC is to provide, in a fashion similar to CAF, efficient access to the underlying machine with common C syntax and semantics.

For vector processing, CAF and UPC support in the compiler is closely integrated with the optimizer. This allows the emitted code to take full advantage of the vector processing's memory architecture for low latency communication.

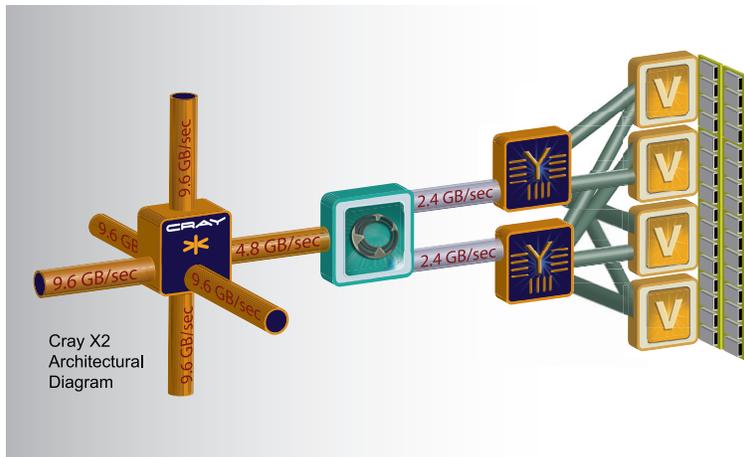
Flexible Processing Options

The revolutionary Cray XT5_n system can incorporate a variety of processor blades, allowing customers to design the ideal supercomputing system for their unique users and environment.

In addition to the AMD Opteron™-based Cray XT4™ and Cray XT5™ blades, the Cray XT5_n system can be supplemented with vector and FPGA processor technologies.

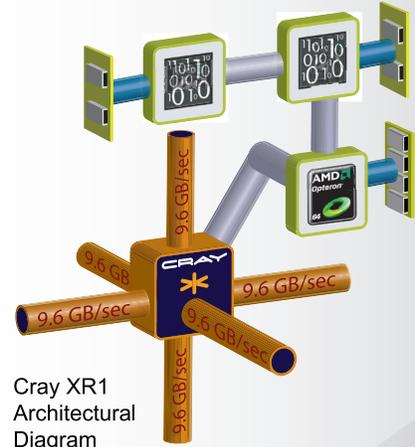
Cray X2™ Vector Processing Blade

The Cray X2 Vector Processing Blade is a single-core, extremely high-bandwidth processing component that provides unique capabilities for applications with memory-intensive workloads and massive data problems to process (for example, applications that use a global address space including UPC and CAF).



Cray XR1™ Reconfigurable Processing Blade

The Cray XR1 Reconfigurable Processing Blade offers the industry's first massively scalable FPGA solution, providing order-of-magnitude performance improvement on certain types of applications. It includes a well-defined software environment to simplify the integration of reconfigurable routines into existing programs, as well as compatibility with common development tools.



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